

CHAPTER 8

8051 HARDWARE CONNECTION AND INTEL HEX FILE

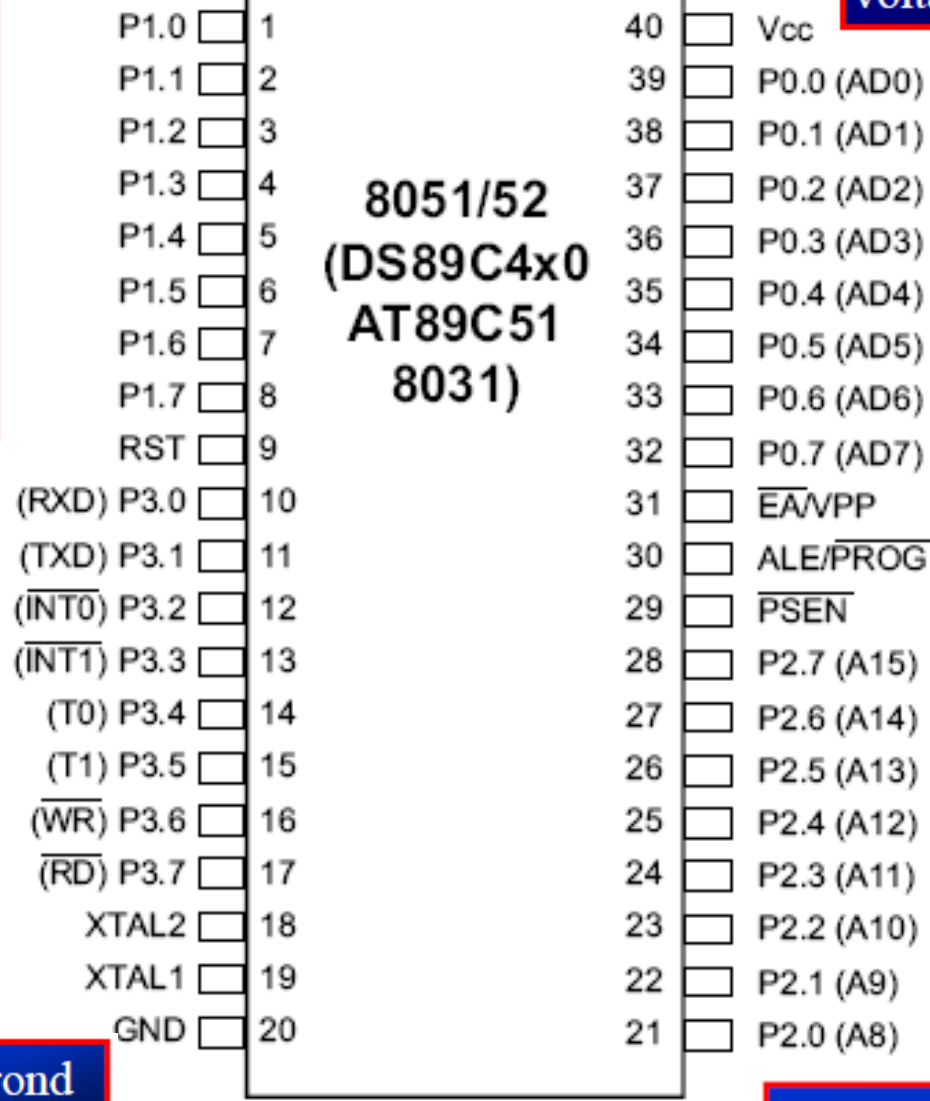
Pin Description

- 805 I family members
 - e.g., 875 I, 89C5 I, 89C52, DS89C4x0)
 - Have 40 pins dedicated for various functions
 - Such as I/O, -RD, -WR, address, data, and interrupts
 - Come in different packages, such as
 - DIP (dual in-line package), QFP (quad flat package), and LLC (leadless chip carrier)
- Some companies provide a 20-pin version of the 805 I with a reduced number of I/O ports for less demanding applications

PDIP/Cerdip

Provides +5V supply voltage to the chip

A total of 32 pins are set aside for the four ports P0, P1, P2, P3, where each port takes 8 pins



Vcc, GND, XTAL1, XTAL2, RST, -EA are used by all members of 8051 and 8031 families

Grond

-PSEN and ALE are used mainly in 8031-based systems

Figure 8-1. 8051 Pin Diagram

XTAL1 and XTAL2

- The 8051 has an on-chip oscillator but requires an external clock to run it
 - A quartz crystal oscillator is connected to inputs XTAL1 (pin 19) and XTAL2 (pin 18)
 - The quartz crystal oscillator also needs two capacitors of 30 pF value

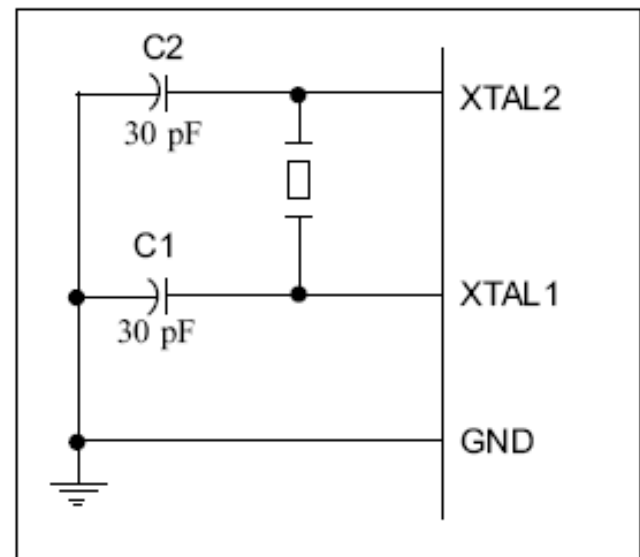


Figure 8-2 (a). XTAL Connection to 8051

XTAL1 and XTAL2 (cont.)

- If you use a frequency source other than a crystal oscillator, such as a TTL oscillator
 - It will be connected to XTAL1
 - XTAL2 is left unconnected

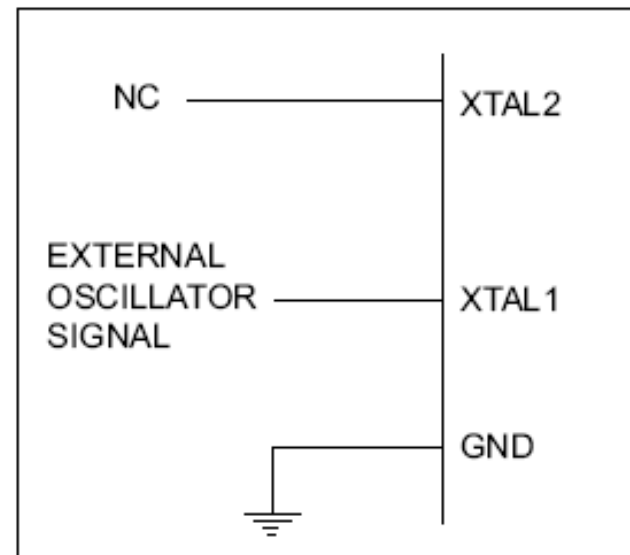


Figure 8-2 (b). XTAL Connection to an External Clock Source

XTAL1 and XTAL2 (cont.)

- The speed of 8051 refers to the maximum oscillator frequency connected to XTAL
 - ex. A 12-MHz chip must be connected to a crystal with 12 MHz frequency or less
 - We can observe the frequency on the XTAL2 pin using the oscilloscope

RST

- RESET pin is an input and is active high (normally low)
 - Upon applying a high pulse to this pin, the microcontroller will reset and terminate all activities
 - This is often referred to as a power-on reset
 - Activating a power-on reset will cause all values in the registers to be lost
 - For the RESET input to be effective, it must have a minimum duration of 2 machine cycles
 - The high pulse must be high for a minimum of 2 machine cycles before it is allowed to go low

RESET value of some 8051 registers

we must place the first line of source code in ROM location 0

Register	Reset Value
PC	0000
DPTR	0000
ACC	00
PSW	00
SP	07
B	00
P0-P3	FF

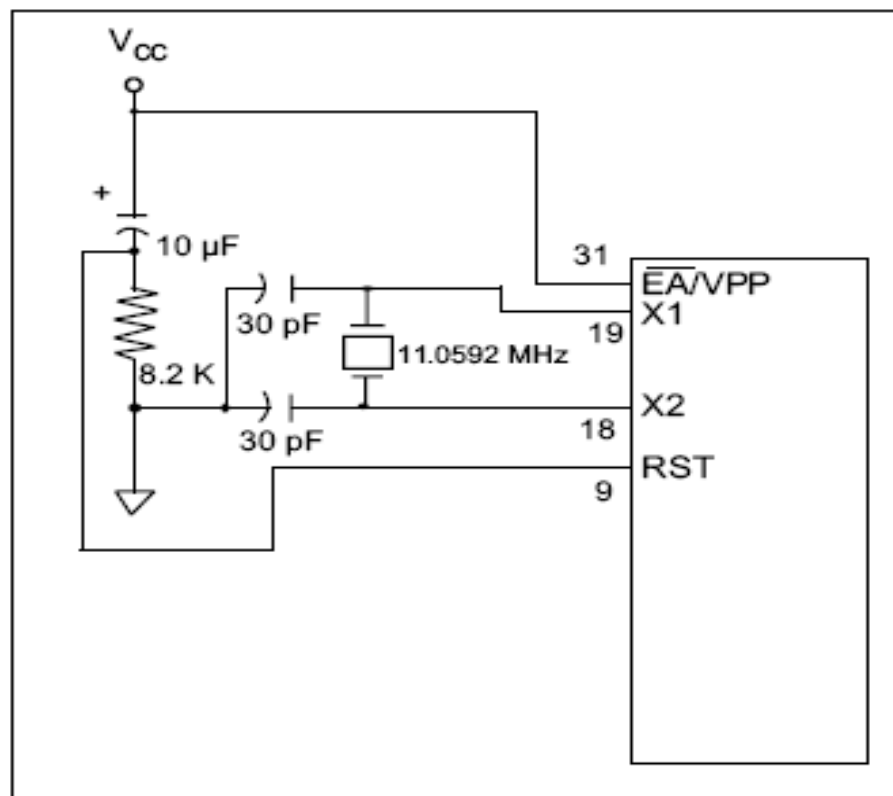


Figure 8-3 (a). Power-On RESET Circuit

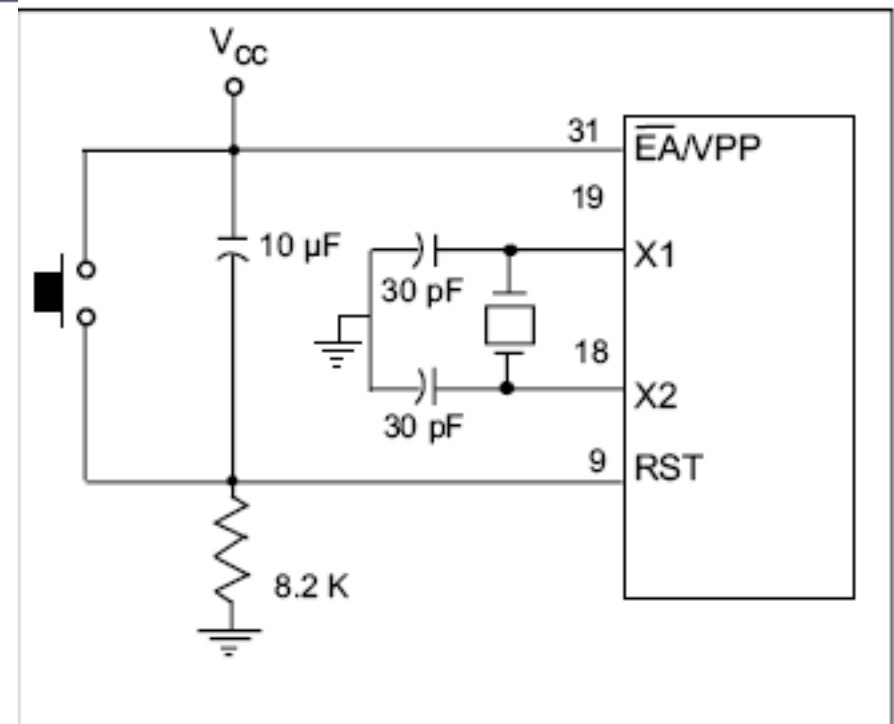


Figure 8-3 (b). Power-On RESET with Momentary Switch

\overline{EA}

- EA, “external access”, is an input pin
 - It must be connected to Vcc or GND
 - The 8051 family members all come with on-chip ROM to store programs
 - EA pin is connected to Vcc
 - The 8031 and 8032 family members do not have on-chip ROM
 - Code is stored on an external ROM and is fetched by 8031/32
 - EA pin must be connected to GND to indicate that the code is stored externally

PSEN & ALE

- Used mainly in 8031-based systems
 - PSEN, “program store enable”, is an output pin
 - This pin is connected to the OE pin of the ROM
 - ALE, “address latch enable”, is an output pin and is active high
 - Port 0 provides both address and data
 - The 8031 multiplexes address and data through port 0 to save pins
 - ALE pin is used for demultiplexing the address and data by connecting to the G pin of the 74LS373 chip

I/O Port Pins

- The four 8-bit I/O ports P0, P1, P2 and P3 each uses 8 pins
- All the ports upon RESET are configured as output, ready to be used as input ports

Port 0

- Port 0 is also designated as AD0-AD7
 - Allowing it to be used for both address and data
 - When connecting an 8051/31 to an external memory, port 0 provides both address and data
 - The 8051 multiplexes address and data through port 0 to save pins
 - ALE indicates if P0 has address or data
 - When ALE=0, it provides data D0-D7
 - When ALE=1, it has address A0-A7

Port 0 (cont.)

- It can be used for input or output
 - Each pin must be connected externally to a 10K ohm pull-up resistor
- This is due to the fact that P0 is an open drain, unlike P1, P2, and P3
 - Open drain is a term used for MOS chips in the same way that open collector is used for TTL chips

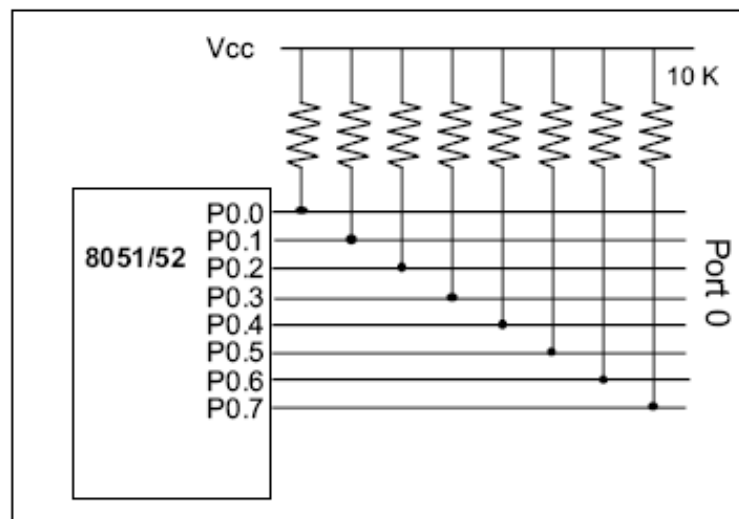


Figure 8-4. Port 0 with Pull-Up Resistors

Port 1 and Port 2

- In 8051-based systems with no external memory connection
 - Both P1 and P2 are used as simple I/O
- In 8031/51-based systems with external memory connections
 - Port 2 must be used along with P0 to provide the 16-bit address for the external memory
 - P0 provides the lower 8 bits via A0 – A7
 - P2 is used for the upper 8 bits of the 16-bit address
 - Designated as A8 – A15
 - It cannot be used for I/O

Port 3

- Port 3 can be used as input or output
 - Port 3 does not need any pull-up resistors
 - Port 3 has the additional function of providing some extremely important signals

P3 Bit	Function	Pin
P3.0	RxD	10
P3.1	TxD	11
P3.2	$\overline{\text{INT0}}$	12
P3.3	$\overline{\text{INT1}}$	13
P3.4	T0	14
P3.5	T1	15
P3.6	$\overline{\text{WR}}$	16
P3.7	$\overline{\text{RD}}$	17

Serial communications

External interrupts

Timers

Read/Write signals of external memories

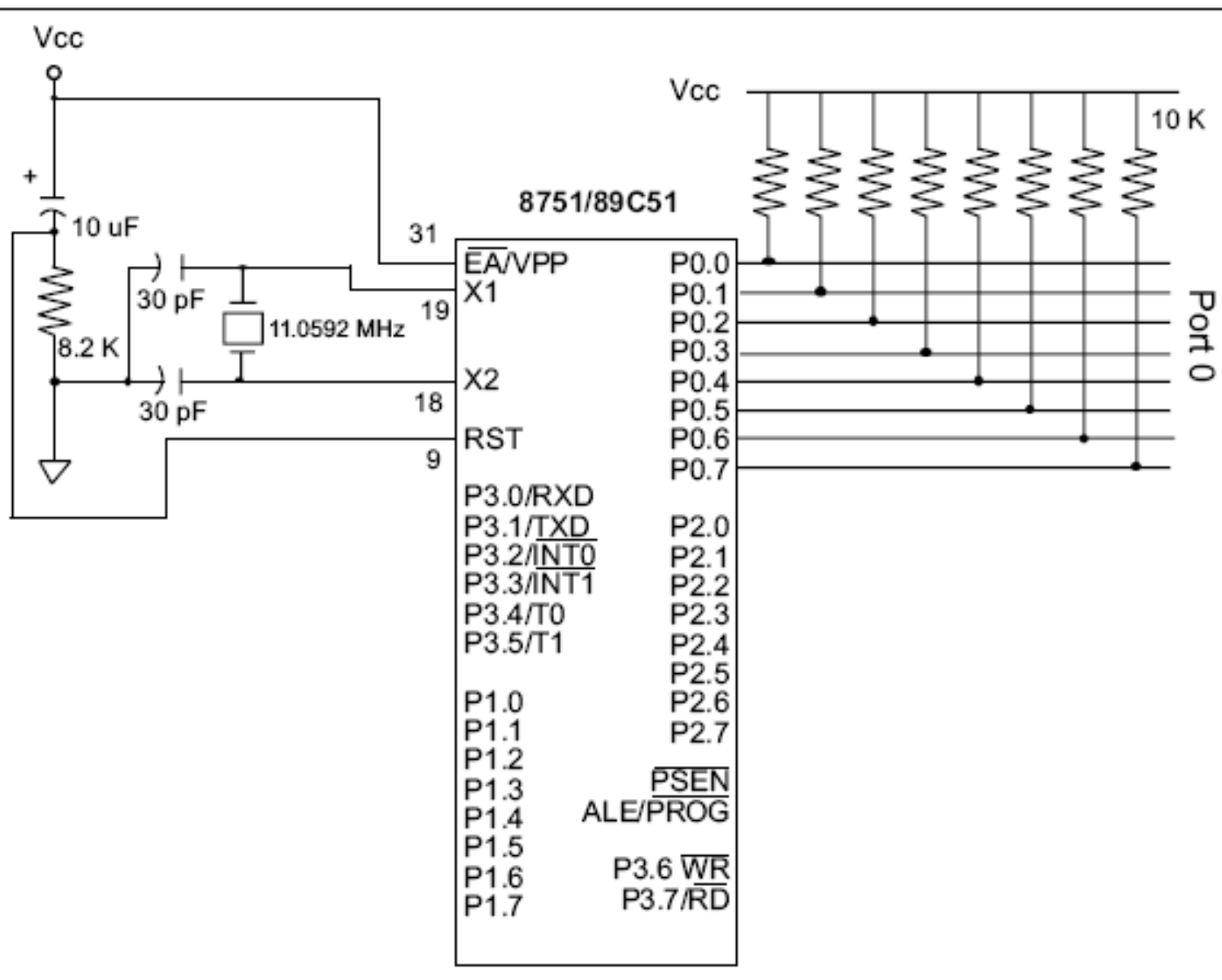


Figure 8-5. Minimum Connection for 89C51/52-Based Systems